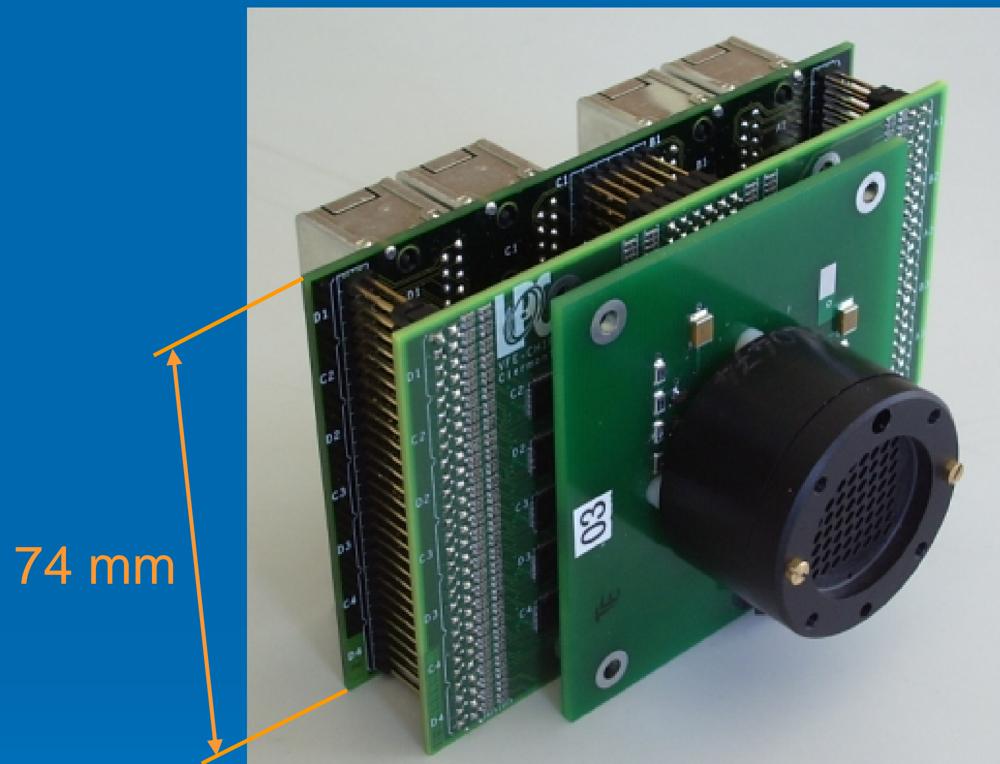
TS/CV/DC CFD Team



Thermal behavior of the LHCb PS VFE Board

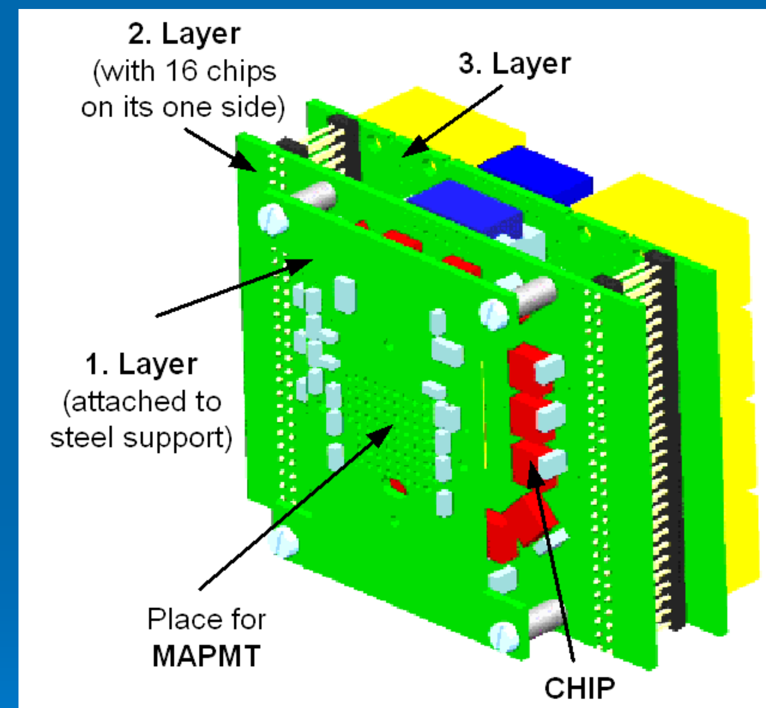
EDMS 624664

Vaclav Vins

THE PROBLEM

- This project was focused on CFD study of small electronics device cooling.

- **Two simulations** of the cooling were considered in this study:
  - **Dry air cooling**
  - **Water cooling**
- PS VFE Board installed at PS part of LHCb Detector consists of three main layers. 16 chips which should be cooled down are installed on bottom side of the second (middle) layer.
- Technical parameters:
  - Heat power in one PS Board … 8 W (0,5 W/chip)
  - Maximum temperature of the chip surface … + 50 C



PS VFE Board

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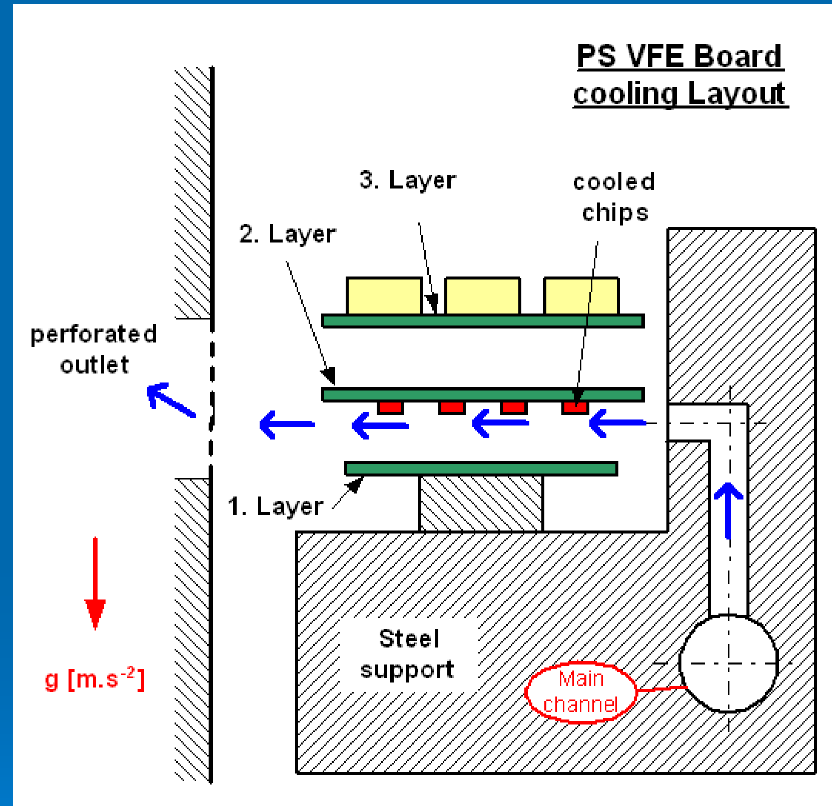
AIR COOLING – MAIN PARAMETERS

PRIMARY SOLVED PARAMETERS:

- Necessary **minimum mass flow rate** of the cooling air
- Optimize position and main dimensions of the air-flow inlets

SOLUTION ASSUMPTIONS:

- Turbulent flow with high Reynolds number was put into account.
- Material of the chips was modeled as pure silicon.
- Produced heat was considered as surface heat source at circuitry area of the die.
- All walls except chip active surfaces were assumed as adiabatic.



Scheme of the air-cooling layout

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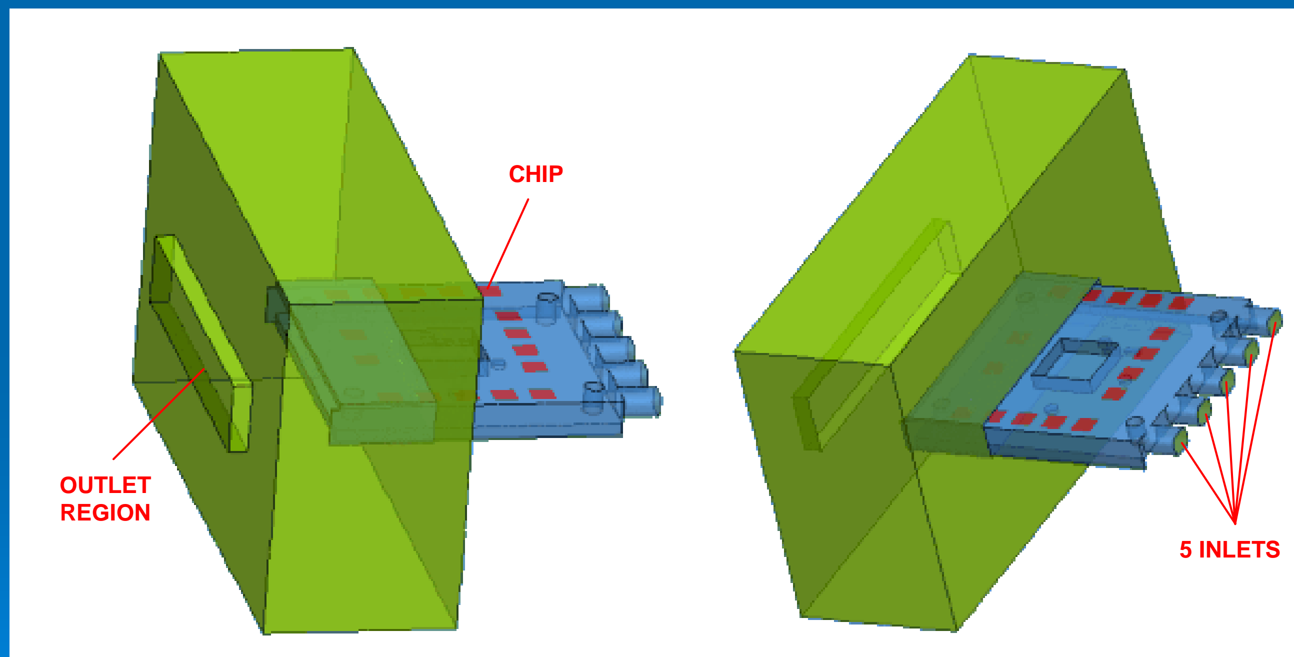
AIR COOLING - CFD MODEL

- Geometry of the problem was defined and simplified on the base of CATIA technical drawing.
- Only the volume area between first and second layer of PS VFE Board and the outlet region was modeled.
- Assumed number of the cells … around **400 000**.



Generated mesh of the problem with tetrahedral cells

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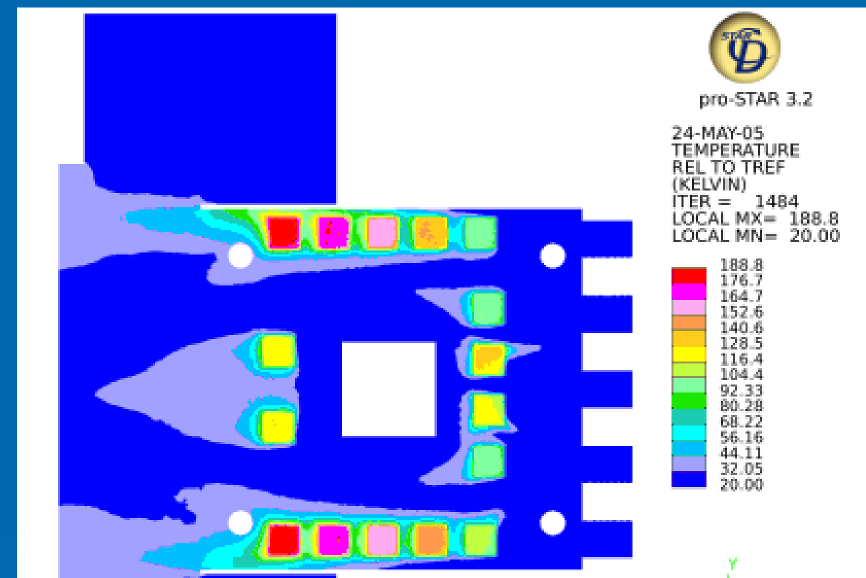
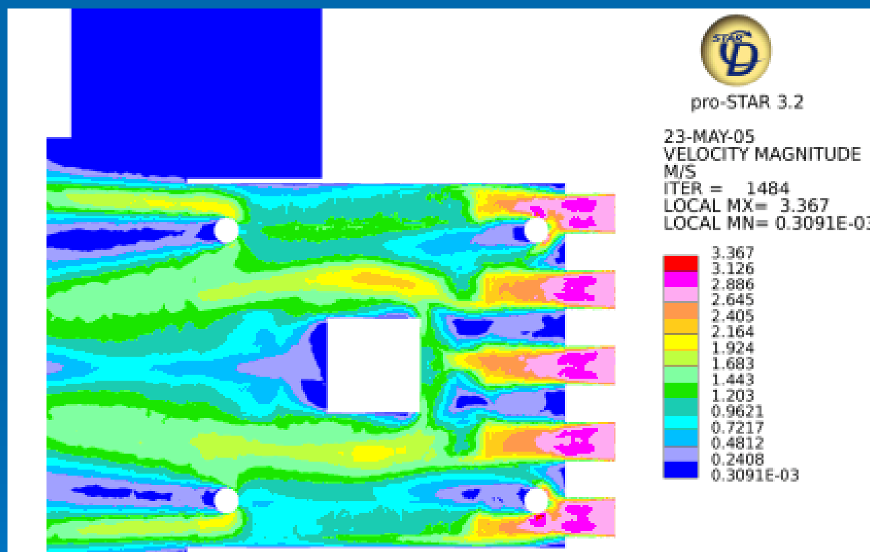
AIR COOLING - RESULTS

- The air-cooling solution was found as more expensive and less effective compared to water cooling.



Cross section of the model with temperature field on the chip free surfaces (m = 0,7 g/s)



Cross section of the model with velocity field of cooling air (m = 0,7 g/s)

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WATER COOLING – MAIN PARAMETERS

PROBLEM DEFINITION:

- In this case the PS Board is cooled with **water** of temperature around + 20°C.
- **Metal block** attached to distributing pipes should remove the heat produced by chips by thermal conduction.
- Effectiveness of the heat transfer between metal block and the chips is improved by **special foil** of thermally conductive interface material.

Due to the symmetry only one half of the area between the first and the second layer of PS Board was modeled. Generated mesh consisted of **350 000** cells.

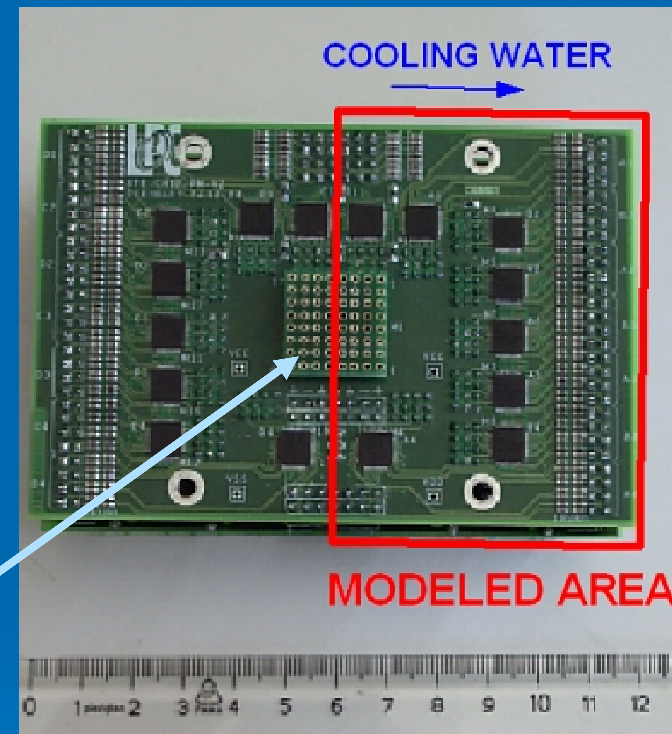

Photo of the second PS Board layer

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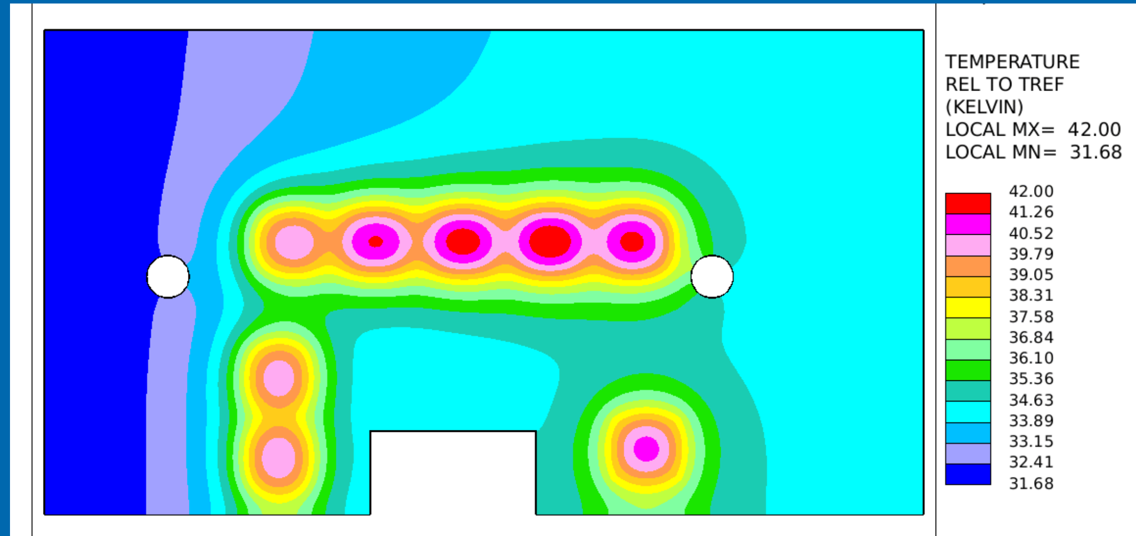
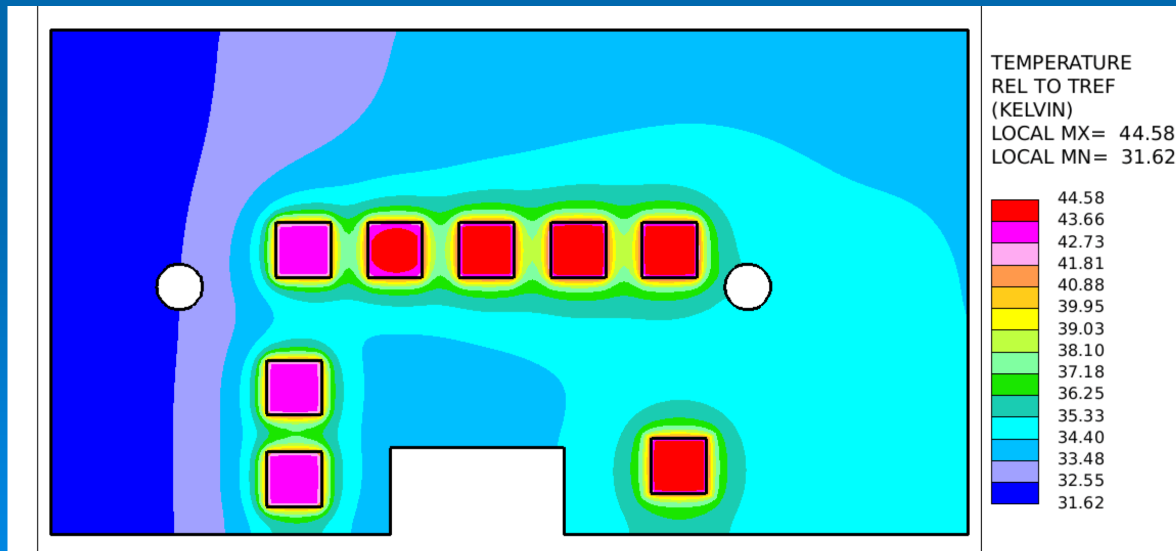
WATER COOLING – RESULTS

Surface temperature of the chips did not reach limit value 50°C.

Obtained results of the temperature field are in a good agreement with experimental data.



Temperature field on the green layer free surface



Temperature field in the cross section area led on the chip upper surfaces

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